Digital Integration

Introduction

When integrating the digital part of modern electronic systems, various technical and financial criteria must be considered. Over 10 years of ASIC experience have shown that no one methodology can meet all requirements at the same time. TEMIC's experience at proposing the most appropriate solution to its customers has resulted in long-term partnerships. Our customers/partners have themselves experienced several ways of completing ASICs, from the use of heavy internal investment with their own design centers, to full sub-contracting to ASIC vendors from product specifications.

Know-how protection, engineering workload management and evolution of merchant CAD tools have been key factors in the evolution of the preferred solutions.

The border between the in-house skills of equipment manufacturers and those of semiconductors makers has evolved: high level behavioral description, such as VHDL, has become the most appropriate language for users to bridge the gap between system description and physical implementation. At the other end of the scale, submicron electronics and faster digital systems have revealed new challenges to cope with the electrical behavior of signals, both on and outside the chip. For instance, clock or signal skews, cross-talks, noise, electromagnetic emission or susceptibility have become the main drivers of first-pass yields in design.

Testing of large integrated systems, sometimes including processor cores, is also a matter of trade-offs between circuit cost, development time and safety operation. New generations of programmable devices such as CPLD or FPGA have also appeared, offering unbeatable flexibility and development time, but with additional cost, sourcing, logistics, and reliability considerations.

In addition to the extensive experience of our designers, TEMIC has developed an unrivalled choice of ASIC solutions offering the best trade-off in development or production cost, flexibility or performance.

Our solutions are also compatible with previous choices or vendor policies from our clients. On top of our proven capacity to deliver high-quality silicon devices in volume, we are recognized for helping our customers to secure their present or future supplies, while remaining competitive for the lifetime of their systems.

TEMIC is committed to providing cost-efficient, technically excellent solutions.

Digital Integration

Cell-Based Designs Optimize Silicon Without Layout Skill

Design stages can be fully completed by the customer from specification to final postlayout simulation. Design rule check (DRC) and layout versus schematic (LVS) are performed by the customer and are its responsibility, unless specific agreement has been reached. Test vectors if applicable are delivered by the customer according to MHS rules.

0.6-µm CMOS Cell-Based Designs

Description

TEMIC calibrated COMPASS cell based tools and libraries on CMOS 0.6-µm process, bring an additional option to its customer base to make designs where:

○ the designer skill doesn't need to be as high as for full custom designs,

○ the density and speed are close to those of a full custom design, while keeping a design cycle close to composite array one.

Features

○ Calibrated on 3 ML, 0.6-µm drawn CMOS technology
○ Set of libraries qualified on COMPASS tools
- MHSC673 symbolic standard cell library
- MHCC6DP1 datapath compiler
- MHCC650 synchronous RAM and ROM compilers
- MHCC62P1 two port RAM and FIFO compiler
- MHCC6RA3 asynchronous RAM compiler

○ Compared to 0.8-µm COMPASS libraries :
- the density is improved by a factor better than 4
- the speed is improved by 40%

○ TEMIC designed blocks can be imported
○ Can be used for MGM1 blocks compilation
○ Addresses designs when :
- either speed and density are of importance
- or quantity to be produced allows NRE to be amortized
- or for existing competition designs conversion
- design modes: 1 or 5

Performances

The compilers can generate the following maximum size functions:

○ asynchronous SRAMs from 128 to 64-K bits with :
- width ranging from 8 to 32 bits,
- depth ranging from 16 to 2048 words.

○ synchronous SRAM from 512 to 16-K bits with :
- width ranging from 8 to 32 bits,
- depth ranging from 64 to 2048 words

○ two port RAM from 128 to 32-K bits with :
- width ranging from 2 to 32 bits in 2 bit increments,
- depth ranging from 64 to 2048 words.

○ ROM from 256 to 128-K bits with :
- width ranging from 4 to 64 bits in 1 bit increment,
- depth ranging from 64 to 4096 words.

Typical performances for some basic functions are demonstrated in the following table:

	Address Access Time (ns)	**Power Consumption (mW/MHz)**	**Size (mm^2)**
2 K x 16 Two Port RAM	12,8	10,76	11
4 K x 32 ROM	21,5	11,12	2,5
2 K x 8 Synchronous RAM	17,2	2,76	2,5
2 K x 32 Asynchronous RAM	10,4	2,4	13

The package offering is similar to MG1M.

0.8-µm CMOS Cell-Based Designs

Description

TEMIC calibrated COMPASS Cell Based tools and libraries on CMOS 0.8 µm, bring an additional option to its customer base to make designs where :

○ the designer skill doesn't need to be as high as for full custom designs,

○ the density and speed are close to those of a full custom design, while keeping a design cycle close to the composite array one.

Features

○ Calibrated on an advanced very low power CMOS process:
- Two metal layers
- 0.8-µm effective channel length for n- and p-transistors
- 12-µm epi wafers

○ MHSC3xx set of libraries qualified on COMPASS tools:
- VSC370 for standard cell, density optimized
- VSC350 for standard cell, speed optimized
- VDP300 for datapath compilation
- VCC300 for logic compilation

○ Design modes: 1 or 5

The package offering is similar to MCM.

Cell-Based Packaging Availability

Pin Count	Package Type										
	Side Brazed	CerDip	PDIL	SO	LCC	PLCC (J)	BGA	CQFP (J) (*)	CQFP (L) (*)	PQFP (L)	PGA
14	○	○	○	○							
16	○	○	○	○							
18	○	○	○	○							
20	○	○	○	○		○					
24	○	○	○	○		○					
28	○	○	○	○	○	○					
40	○	○									
44					○	○		○		○	
48	○	○									
52						○				○	
64	○										
68					○	○		○			○
80									○	○	
84					○	○		○			○
100									○	○	○
120											○
128									○	○	
132									○		○
144							C				○
160									○	○	
176											○
196							C		○		
204							C				
208										○	
209											○
240							C			C	
256											○
304										C	
323											C
336							C				
384							C				

C = Check for availability

(*) Consult factory for RT version – MQFL package is preferred

Customer and TEMIC Design Flows

Design Offering

Five different ASIC design offerings are available: ULC, Gate Arrays, Composite Arrays, Cell Based and Full Custom. Each physical implementation gives an answer to the compromise: flexibility/unit price and integration/development cost.

Design Modes

Three different design modes can be agreed upon between the customer and TEMIC, depending on system and integration skills requirements.

Mode	Logic Design	Physical Layout	Design Tools
Customer Design	Customer	Customer	Customer tools
Customer and TEMIC Design	Customer	TEMIC	TEMIC supported tools[a] (Netlist and simulation)
TEMIC Design	TEMIC	TEMIC	TEMIC supported tools[a] (Netlist and simulation)

a. Supported tools are currently CADENCE, COMPASS, MENTOR, SYNOPSYS and VHDL/VITAL.

Design Modes versus Design Offering

Mode / Product Family	Customer Design	Customer and TEMIC Design	TEMIC Design
ULC			□
Gate Array		x	□
Composite Array		x	□
Cell Based	x	○	□
Full Custom	x		□

x : standard offer.
○ : dependant on human and hardware resources needed and/or available.
□ : specific development using TEMIC own expertise.

Design Phases and Meetings

The design of a circuit is separated into four main phases, separated by three major meetings between TEMIC and the Customer, as shown in Figure 1.

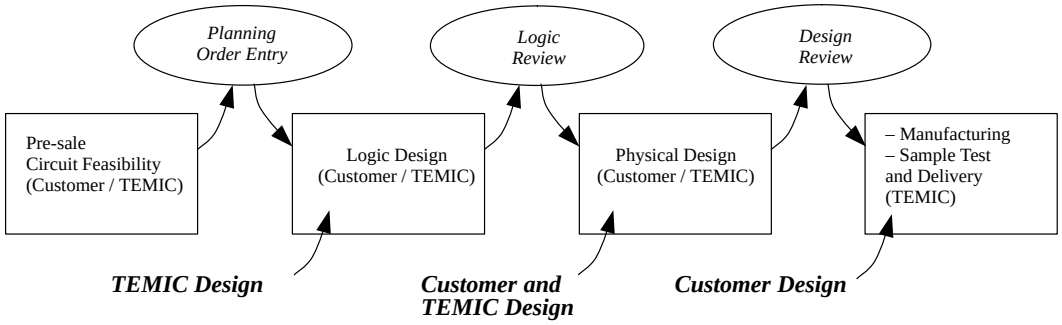

Figure 1. The Design Phases and Meetings

Technology for Digital Integration

Description

TEMIC develops a wide range of CMOS technologies, used for catalog products or ASICs' in volume production. Their common features are high performance/high speed both with low power consumption, either in stand-by or operating modes.

TEMIC makes these technologies available for selected customers/partners for their own design.

Features

TEMIC technologies include digital CMOS technologies and several derivatives from the CMOS core basis:

- mixed analog/digital series with one more polysilicon layer and low V_t transistors
- non-volatile series with high voltage NMOS transistors and programming/sensing/erasing capabilities
- radiation tolerant process with specific guard rings

	Technology	Well	Lithography (µm)	Poly Layers	Metal Layers	Operating Voltage (V)	Characteristics
Digital Series							
FCC1D	CMOS	N	0.8	1	2	5 or 3	
FCC1S	CMOS	N	0.8	1	1	5 or 3	
FCC2D	CMOS	Twin	0.6	1	2	5 and/or 3	
FCC2T	CMOS	Twin	0.6	1	3	5 and/or 3	
FCB1D	BICMOS	Twin	0.8	1	2	5 and/or 3	NPN
Mixed Analog/Digital Series							
FCA1D	CMOS	N	0.8	2	2	5 and/or 3	Low V_t
FCA2D[a]	CMOS	N	0.6	2	2	5 and/or 3	
FCA2T[a]	CMOS		0.6	2	3	5 and/or 3	
Non Volatile Series							
FCN1D	CMOS	2	0.8	1	2	5	EPROM
FCN2T[a]	CMOS	2	0.6	1	3	5 and/or 3	EPROM
Radiation Tolerant Series							
FCT1D	CMOS	N	0.8	1	2	5	Guard Ring
FCBTD	BICMOS	Twin	0.8	1	2	5	Guard Ring
FCT2D	CMOS	Twin	0.6	1	3	5 and/or 3	Guard Ring

a. Planned